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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,341	01/16/2002	Christian Panis	1406/39	6236

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EXAMINER
KIM, KENNETH S

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 12/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/050,341	PANIS, CHRISTIAN	
	Examiner	Art Unit	
	Kenneth S KIM	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

KENNETH S. KIM
PRIMARY EXAMINER

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1- 7 remain for examination.

2. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Kurosawa et al, U.S. Patent No. 5, 287,465, cited in the previous office action.

The rejection is respectfully maintained for the reason set forth in the previous office action incorporated herein by reference.

The reference states,

(in the abstract)

> Further, the **parallel** processing apparatus making great account of compatibility of a great part of software reads out m instructions without using the processing state flag, decodes the m instructions, *checks whether a branch instruction exists in the k-th instruction, then executes* ***the first to the (k+1)-th instructions in k+1 arithmetic units, and prevent execution of the (k+ 2)-th to m-th instructions.*** By executing the k-th branch instruction, the parallel processing apparatus calculates an address nm+h of its branch destination, performs calculation to check whether the condition is satisfied or not, then prevents execution of instructions of addresses nm to nm+h-1, and executes instructions of addresses nm+h to (n+1)m. In this way, the parallel processing apparatus executes a plurality of instructions and successively executes branch instructions. [Emphasis added]

(in the specification page 4, line 61 – page 5, line 34)

> In accordance with a second feature of the present invention, a **parallel** processing apparatus comprises a program counter for indicating an instruction to be read out, m instruction registers for storing indicated instructions therein, a register file for storing data therein, arithmetic units sharing the register file and executing an arithmetic operation, *plural instructions parallel processing means for reading m consecutive instructions* from an address indicated by the program counter **and for processing these m instructions in m arithmetic units**, conditional branch instruction processing means having a conditional branch instruction and an unconditional branch instruction and preventing execution of instructions located after an address of a delayed slot instruction immediately succeeding a conditional branch instruction upon satisfaction of the condition of the conditional branch instruction included in m instructions read out by the program counter, and unconditional branch instruction processing means for preventing execution of instructions located after an address of a *delayed slot instruction* immediately succeeding an unconditional branch instruction upon presence of the unconditional branch instruction in the m instructions read out by the program

> counter. In such configuration, **m instructions are first read out and decoded to check if there is a branch instruction in the k-th instruction. Succeedingly, *the first to the (k+1)th instructions are executed in the (k+1)th arithmetic unit*, and execution of the (k+2)th to the m-th instructions is prevented.** By executing the k-th branch instruction, address nm+h of the branch destination is calculated and calculation for checking whether the condition is satisfied or not is performed. Succeedingly, m instructions are read out from address nm. Execution of instructions ranging from the address nm to address nm+h-1 is then prevented, and instructions ranging from the address (nm+h) to address (n+1)m are executed. As a result, **a plurality of arithmetic units operate in parallel, and hence a plurality of instructions can be efficiently executed.** In addition, branch instructions can also yield the same processing results as those of successive execution. [Emphasis added]

Thus, the reference discloses execution of m instructions in m arithmetic units in parallel, wherein if k-th instruction is a branch instruction, (k+2)th to m-th arithmetic units are prevented from executing (k+2)th to m-th instructions.

Although the specification makes a typographical error in stating "the first to (k+1) instructions are executed in the (k+1)th arithmetic unit", it is apparent from the context of the disclosure and from the abstract that - - the first to (k+1) instructions are executed in (k+1) arithmetic units- - is intended. [If k-th instruction is a branch instruction, then (k+1)th instruction is a delay slot instruction that is executed along with the first to (k-1)th instructions.]

3. Applicant's arguments filed October 29, 2004 have been fully considered but they are not persuasive.

Applicant argued that the reference teaches only one (k+1)th arithmetic unit executing instructions (relying on the portion with a typographical error), and hence, does not teach parallel execution of commands by a number of processors.

Examiner believes that, notwithstanding the typographical error, the reference teaches parallel processing of commands by a plurality of processors (first to k+1 arithmetic units) as noted above.

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth S KIM whose telephone number is (571) 272-3627. The examiner can normally be reached on M-F (8:30-17:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

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December 3, 2004

KENNETH S. KIM
PRIMARY EXAMINER